Freescale Semiconductor
Hardware Getting Started Guide

Document Number: P5040 DS_HGS
Rev. 1.5

P5040 DS (SuperHYDRA)

This document describes the P5040 DS (SuperHYDRA) and its related hardware kit. The P5040 DS (SuperHYDRA) Getting Started procedure explains and verifies basic board operation in a step-by-step format.

Settings for switches, connectors, jumpers, push buttons, and LEDs are shown, and there are instructions for connecting peripheral devices.

The P5040 DS (SuperHYDRA) functions with an integrated development environment (IDE), such as Freescale's *CodeWarrior* ™; however, instructions for working with the IDE are beyond the scope of this document.

Contents

freescale™ semiconductor

1 Revisions Table

Table 1. Revisions Table

Date	Rev.	Author	Tech Editor	Description
Dec 2011	1.0	Vladimir Yukht & Limor Peretz		HWGS Rev. 1.0
Jan 2012	1.1	Vladimir Yukht & Limor Peretz		HWGS Rev. 1.1
Jan 2012	1.2	Vladimir Yukht & Limor Peretz		“Programming model” paragraph removed (See User Guide for details)
March 2012	1.21	Vladimir Yukht & Limor Peretz		P5021 device setting added
March 2012	1.22	Vladimir Yukht & Limor Peretz		Photo’s are updated. Ref. clocks default setting added
May 2012	1.3	Vladimir Yukht & Limor Peretz		Default SYSCLK for P5040 changed to 100MHz
July 2012	1.4	Vladimir Yukht & Limor Peretz		Default SYSCLK and PDN option for P5040 changed to 133MHz & CA+CB -Common; PL - Independent. P5021 & P5010 devices setup added
Oct 2012	1.5	Vladimir Yukht & Limor Peretz		Optional DDR_RST program control added. FPGA OCM/DCM updated

2 Acronyms and Abbreviations

Table 2.

Usage	Description
ACK	Acknowledge
ADDR	Address
ARCH	Architecture
ATX	Advanced Technology Extended (power supply)
AURORA	Aurora Systems
AUX	Auxiliary
AVDD	Address Bus Voltage
BRDCFG	Board Configuration
BVDD	Local Bus Direct Current Voltage

Table 2.

Usage	Description
CA	Core A
CB	Core B
CC	Core Cluster
CFG	Configuration
chkstpi	Checkstop In
CLK	Clock
CLKIN	Clock Input (interchangeable with SYSCLK)
CLKSPREAD	Clock Spread
CNTL	Control
COP	Common On-Chip Processor
CPU	Central Processing Unit
CSR	Control Status Register
CVDD	Clock Driver Supply Voltage / Bus Control Voltage
CW	CodeWarrior
DBGSEL	FPGA GMSA GMDBG Register Select
DDR	Double Data Rate
DIP	Dual-In-Line Package (switches)
DIR	Direction
DIS	Disable
DRAM	Dynamic Random Access Memory
DS	Development System
EC	Chip HW Specification
ECC	Error Detection and Correction
eDINK	e500 core Demonstrative Interactive Nanokernel
EEPROM	Electrically Erasable Programmable ROM
eLBC	Enhanced Local Bus Controller
EMI	ElectroMagnetic Interference
eMMC	Embedded Multi Media Card
EN	Enabled
ENG	Engineering
EP	End Point

Table 2.

Usage	Description
eSDHC	Enhanced Secure Digital High Capacity Card
esig	Internal/Event Signal p. 35
ETH	Ethernet
EVEDEST	Event Destination
EVESRC	Event Source
evt	event
FBSEL	Feedback Select
FCM	NAND Flash Control Machine
FLASHCS	Flash Chip Select
Fman	Frame Manager
FPGA	Field Programmable Gate Array
FSEL	Frequency Select
GEN	Generate
GETH	Giga Ethernet (GbE)
GPINPUT	General Purpose Input
GPIO	General Purpose In/Out
GVDD	Gate Turn-On Voltage / GPIO Voltage
Host	P3041/P5020
HRESET	Hard Reset
HSTAT	Hydra Status
HW	Hardware
HWGS	Hardware Getting Started
I^2C	Inter-Integrated Circuit Multi-Master Serial Computer Bus
ICS307	System Clock Generator
ID	Identification
IDE	Integrated Development Environment
IO	Input/Output
IPL	Initial Program Load
ISOL	Isolated
JTAG	Joint Test Access Group (IEEE® Std. 1149.1™)
LBMAP	Local Bus Map

Table 2.

Usage	Description
LED/LD	Light-emitting Diode
LP	Low Power
LSB	Least Significant Bit
LVDD	P5040 DS (SuperHYDRA) GETH (Low) Voltage
MII	Media Independent Interface
MMC	Multi-media Card
MSB	Most Significant Bit
MUX	Multiplexer
NAND	Flash Memory
NDA	Non-Disclosure Agreement
NG/ng	New Generation; e.g., ngPIXIS
NOR	Flash Memory
NVIDIA	NVIDIA Corporation
OCM	Off-line Configuration Manager (FPGA-embedded)
OCMCSR	OCM Control/Status Register
OCMMSG	OCM Message
OPT	Option
OVDD	Output Voltage
PCIe/PEX	PCIe = PCI Express = PEX
PG	Power Good
PHY	Physical Layer
PIXISOPT	PIXIS Option
PJWP	PROMJet Write Protect
PL	Platform
PLL	Phased Lock Loop
POVDD	Parameter Operating Voltage
ppm	Parts per Million
PROC ISO	Processor Isolated
PROC SEL	Processor Select
PROMJet	Memory Emulator by EmuTec Inc.
PROMJet Flash	Flash by EmuTec Inc.

Table 2.

Usage	Description
PS	Power Supply
PWR	Power
QorIQ	Brand of power architecture based on a Freescale communications micro controller.
R	Read
RC	Root Complex
RCW	Reset Configuration Word
REF	Reference
REF CLK	Reference Clock (Clock Synthesizer Input Value)
REG	Register
REG CFG	Configuration Register
REQ	Request
RGMII	Reduced General Media Independent Interface
RM	Reference Manual
ROM	Read Only Memory
RSP	Response
RST	Reset
RTC	Real-time Clock
SATA	Serial Advanced Technology Attachment
SCL/SCLK	Serial Clock
SCVER	System Control Version
SD	Secure Digital Card
SDHC	Secure Digital High Capacity
SDREFCLK	SerDes Reference Clock
SEL	Select
SERCLK	SerDes Clock
SerDes (SRDS)	Serializer/Deserializer; e.g., PEX, XAUI, SGMII, SATA, sRIO, AURORA
SGMII	Serial Gigabit Media Independent Interface
SHDN	Shutdown
SMB	Subminiature Version B Connector
SPD	Speed

Table 2.

Usage	Description
SPI	Serial Peripheral Interface Flash
SPICS	SPI Chip Select
SRAM	Static Random Access Memory
STAT	Status
SVDD	Supply Voltage
SVR	System Version
SW	Switch
SXSLOT	SGMII/XAUI Riser Card Slot
SYSCLK	System Clock
TAP	Telocator Alphanumeric Protocol; e.g., USB TAP or ETH TAP
TESTSEL	Test Select
trig/TRIG_IN/OUT	Trigger In/Out
U	Unassigned
UART	Universal Asynchronous Receiver/Transmitter
uDIMM	Unbuffered Dual In-Line Memory Module Form Factor
USB	Universal Serial Bus
USBCLK	USB Clock
V	Volt
VCTL	VELA Control
VDD	Voltage Drain
VELA	VELA Corporation
VER	Version
VSTAT	VELA Status
W	Write
WDEN	Watchdog Enable
WP	Write Protect
WVAL	Watchdog Value
XAUI	Ten Attachment Unit Interface
XVDD	Phased Lock Loop Voltage

3 Related Reading

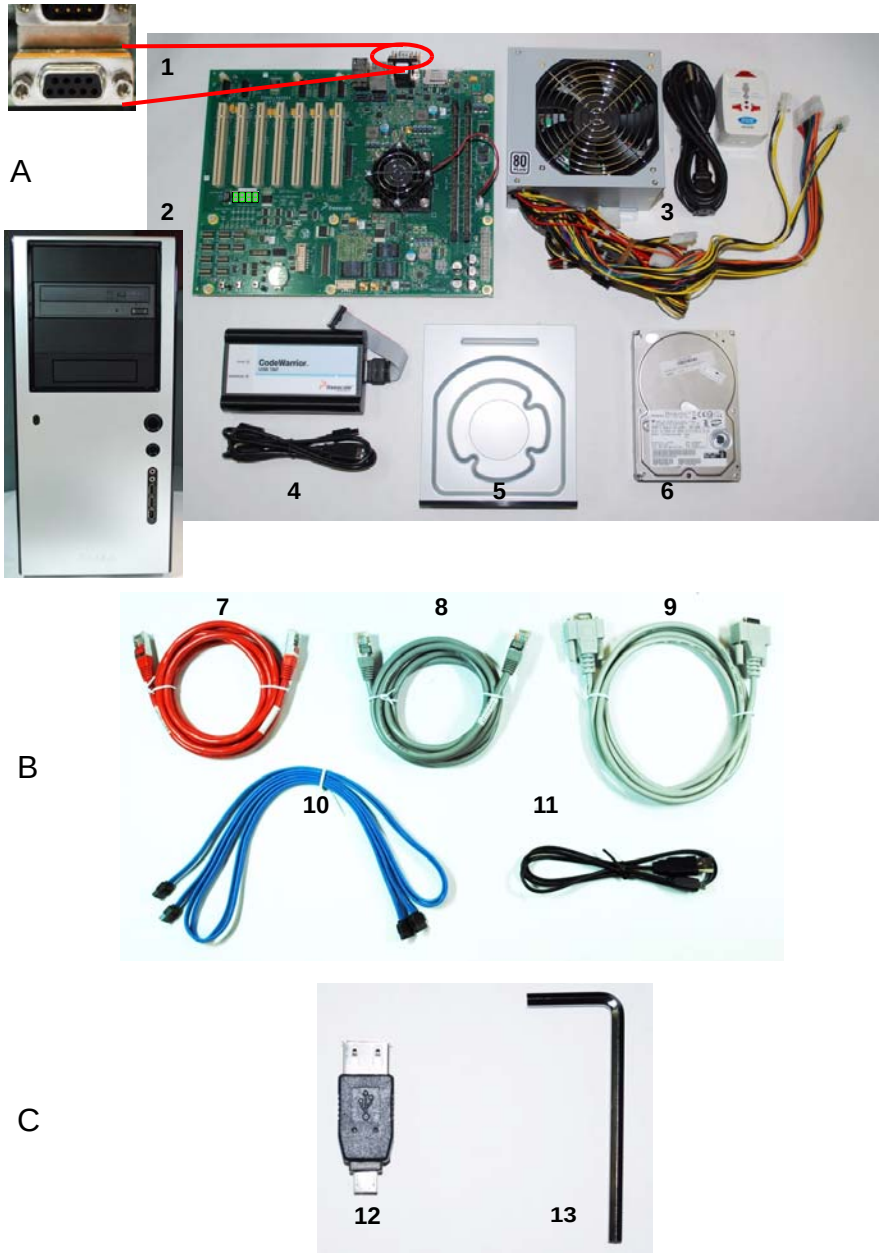
The documents listed in the below table are available via the Freescale website to those with NDA access. The website is found at http://www.freescale.com/.

Table 3. Related Reading

Document	Description
CodeWarrior™ Kit Configuration Guide	• Complete HW setup explanation. • Kit Configuration Guide explains how to set up and use each SW component in the development kit.
P5040 QorIQ Integrated Multicore Communication Processor Family Reference Manual	P5040 RM
P3041 QorIQ Integrated Multicore Communication Processor Family Reference Manual	P3041 RM
P5020 QorIQ Integrated Multicore Communication Processor Family Reference Manual	P5020 RM
P5040 QorIQ Integrated Processor Hardware Specifications	P5040EC
P3041 QorIQ Integrated Processor Hardware Specifications	P3041 EC
P5020/P5010 QorIQ Integrated Processor Hardware Specifications	P5020 EC
Hydra DS SerDes Support	All P3041/P5020DS SerDes support options.
P5040 DS SerDes Support	All P5040DS SerDes support options.
Intersil ISL6313B Datasheet	Two-Phase Buck PWM Controller with Integrated MOSFET Drivers for Intel VR11 and AMD Applications
P5040 DS (Super Hydra) HWUG	Super Hydra User Guide

4 Hardware Kit Contents

This section lists and depicts (see Figure 1) HW kit contents.

HW Kit Inventory	Figure 1. HW Kit Contents
Photo A: Board and External HW 1. P5040 DS (SuperHYDRA) board (1) with connected DB9 Cross Gender adapter (1) 2. PC Mid-Tower 3. ATX PS 12V 600W (1) and US/Canada cable & PS adapter 4. CodeWarrior USB TAP (1 kit) 5. DVD/CD: SATA2 (1) 6. HD: 160GB SATA (1) **Photo B: Cables** 7. ETH cross-over cable with RJ45 connector (1) 8. ETH shielded cable with RJ45 connector (1) 9. RS-232 standard serial cable with two 9-pin connectors (1) 10. SATA cable with 7-pin connector (2) 11. USB*A-to-MicroUSB*B cable (1) **Photo C: Miscellaneous** 12. Micro USB*A-to-USB*A adapter (1) 13. Allen key (1) **NOTE!** Standalone version does not include the PC Mid-Tower, DVD/CD, and HD—marked as numbers 2, 5, and 6, respectively.	

PRINTED MATTER (not shown in Figure 1):

- P5040 DS (SuperHYDRA) HW Getting Started
- Freescale Warranty Card: 920-75133
- Safety Notice: 926-75254
- Contact Information Sheet: 920-90570-00

5 P5040 DS (SuperHYDRA) Component and Print Side Views

Figure 2 shows the component side and Figure 3 shows the print side of P5040 DS (SuperHYDRA).

Figure 2. P5040 DS (SuperHYDRA) Component Side View

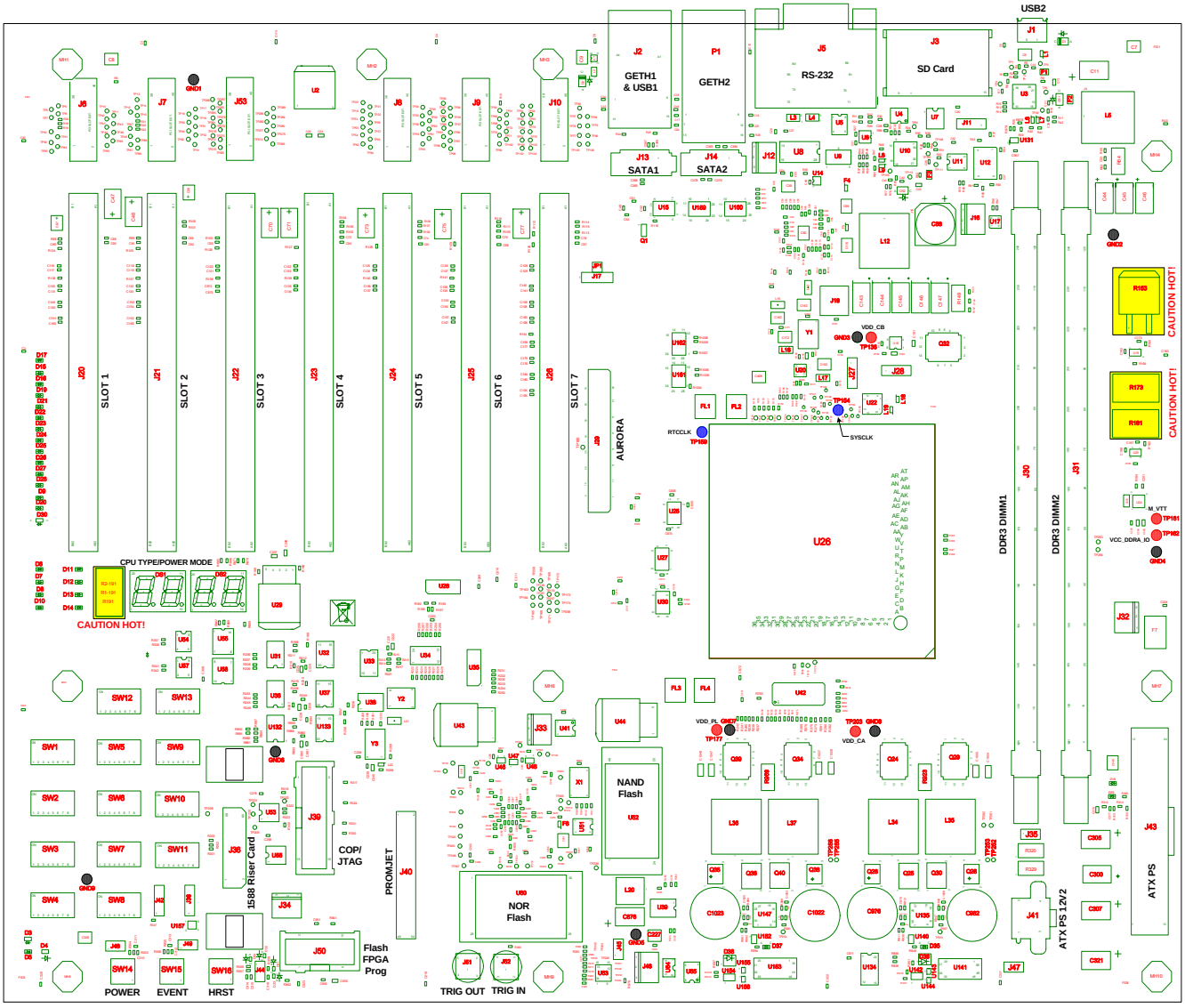
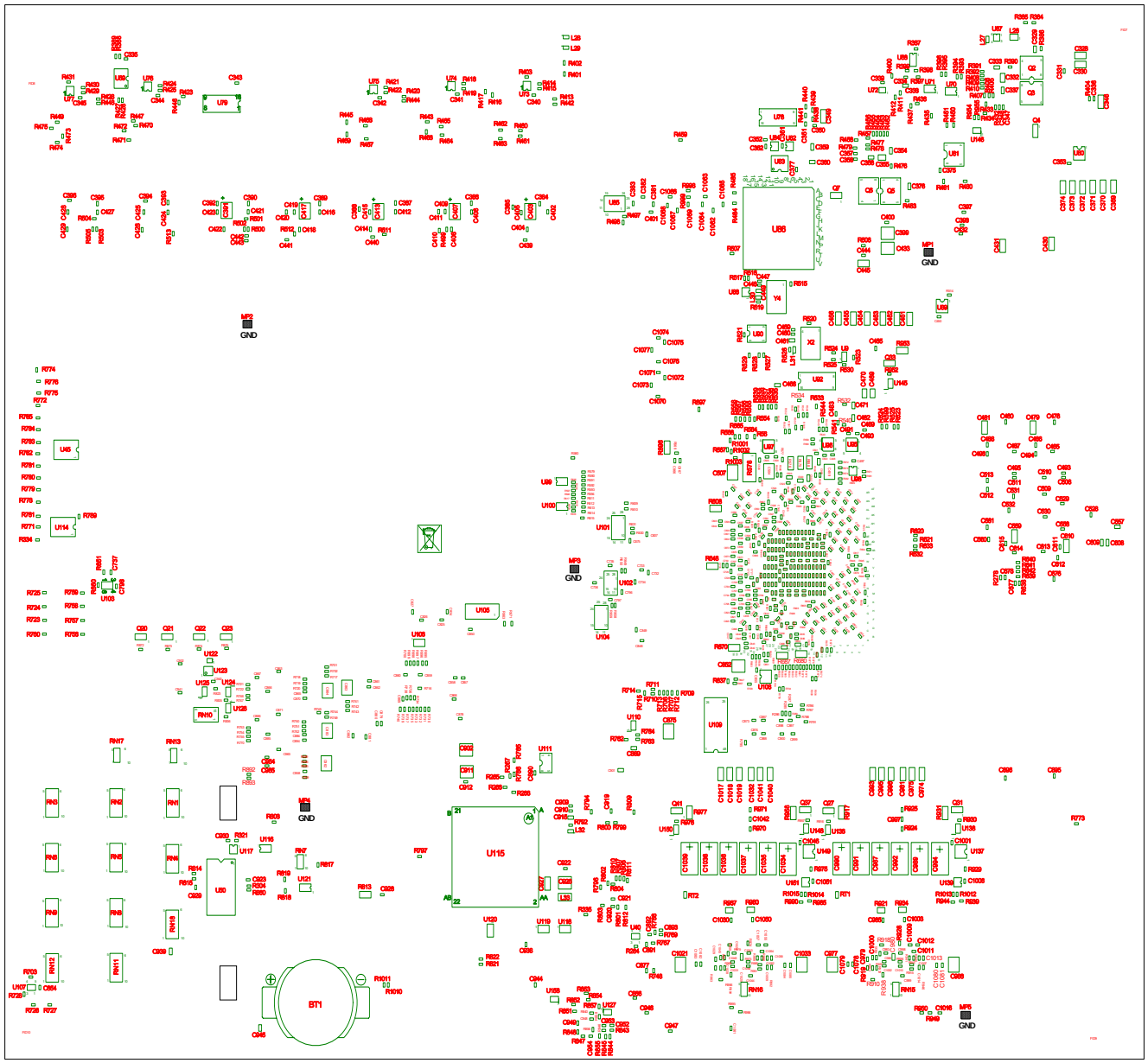


Figure 3. P5040 DS (SuperHYDRA) Print Side View



6 Switch Default Settings

Default DIP-switch positions establish the P5040 DS (SuperHYDRA) mode; see Table 5.

NOTE!

Ensure DIP-switches are set according to default values.

Table 4. P5040 DS (SuperHYDRA) Default Configurations

Mode	Term	Default Value	Unit
AVDD_CC1, AVDD_CC2, AVDD_PLAT, AVDD_DDR	PLL's Supply Voltages (Core, Platform and DDR)	1.05 for P3041/P5020 1.0 for P5040	V
AVDD_SRDS1, AVDD_SRDS2, AVDD_SRDS3	SERDES PLL's Supply Voltages (Filtered from SVDD)	1.05 for P3041/P5020 1.0 for P5040	V
BVDD Voltage	eLBC Block Supply Voltage	3.3 only	V
Core Clock	Depends on RCW	2260 (P5040) / 2000 (P5020/P3041)	MHz
CVDD Voltage	SPI & SDHC Blocks Supply Voltage	3.3	V
DDR CLK	Depends on RCW	800 (P5040) / 666 (P5020/P3041)	MHz
Fman CLK	Depends on RCW	600	MHz
GVDD Voltage	DDR DRAM I/O Supply Voltage	1.5	V
LVDD Voltage	Ethernet EMI1, 1588, GPIO Voltage	2.5	V
OVDD Voltage	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	3.3	V
Platform Clock	Depends on RCW	800	MHz
POVDD Voltage	Fuse programming override supply Voltage	"0"- Default 1.0/1.5	V
RTC CLK	Real-time Clock	~50	KHz
SerDes REF CLK1	SerDes Reference Clock 1	100	MHz
SerDes REF CLK2	SerDes Reference Clock 2	125	MHz
SerDes REF CLK3	SerDes Reference Clock 3	125	MHz
SerDes REF CLK4	SerDes Reference Clock 4	125 (P5040 only)	MHz
SVDD Voltage	Core power supply for SerDes transceivers Voltage	1.05 for P3041/P5020 1.0 for P5040	V
SYSCLK (Synthesizer REF CLK)	System Clock	133.333 (P5040/ P5020)/ 83.333 (P3041)	MHz
USB_VDD_1P0	USB PHY PLL supply Voltage	1.0	V

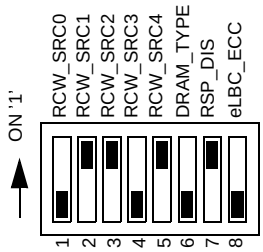
Table 4. P5040 DS (SuperHYDRA) Default Configurations

Mode	Term	Default Value	Unit
USB_VDD_3P3	USB PHY Transceiver supply Voltage	3.3	V
VDD_CA Voltage	Cores Group A supply voltage (not used for P3041)	1.1 for P5020/P5040	V
VDD_CB Voltage	Cores Group B supply voltage (not used for P3041)	1.1 for P5020/P5040	V
VDD_LP Voltage	Low Power Security Monitor Supply	1.0	V
VDD_PL for P5020/P5040 VDD_PL_CA_CB for P3041 Voltage	Platform/Combined Supply Voltage	1.05 for P5020/P3041 1.0 for P5040	V
XVDD Voltage	Pad power supply for SerDes transceivers Voltage	1.8	V

Table 5 provides schematic drawings and related switch descriptions.

Table 5. SW Configurations

SW1 Configuration



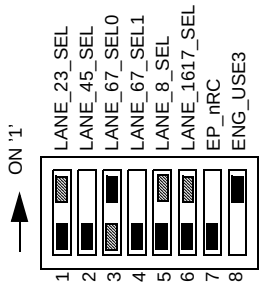
SW1.1 – SW1.5: RCW_SRC[0:4]
(RCW Configuration Source)

Defines RCW configuration sources [0:4] as per P3041/P5020 RM.

Reset Configuration Name	Value (Binary)	RCW Source
cfg_rcw_src[0:4]	0_0000	I^2C1 normal addressing (supports ROMs up to 256 bytes)
	0_0001	I^2C1 extended addressing
	0_0010	Reserved
	0_0011	Reserved
	0_0100	SPI 16-bit addressing
	0_0101	SPI 24-bit addressing
	0_0110	eSDHC
	0_0111	Reserved
	0_1000	eLBC FCM 8-bit small page (512-byte page) NAND Flash
	0_1001	eLBC FCM 8-bit large page (512-byte page) NAND Flash
	0_1010	Reserved
	0_1011	Reserved
	0_1100	eLBC GPCM 8-bit NOR Flash
	0_1101	eLBC GPCM 16-bit NOR Flash **(Default)**
	0_1110	eLBC GPCM 32-bit NOR Flash
	0_1111	Reserved
	1_0000–1_1011	Hard-coded RCW options (See Section 4.4.4.2, "Hard Coded RCW Options," for more information.)
	1_1100–1_1111	Reserved

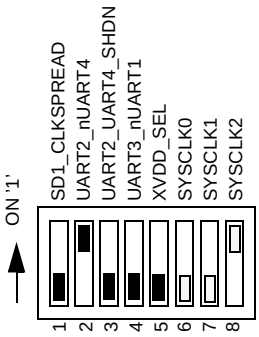
Defines RCW configuration sources [0:4] as per P5040 RM.
Here should be the Table for P5040

	SW1.6: DRAM_TYPE **(DDR RAM Type)** Defines POR DRAM type (DDR3/DDR3L). • **'0' - 1.5V DDR3 technology [Default]** • '1' - 1.35V DDR3L technology **SW1.7: RSP_DIS** **(Response Disable)** Defines functionality. • '0' - RESET pauses at RCW • **'1' - Continued Boot [Default]** **SW1.8: eLBC_ECC** **(Enhanced Local Bus Controller & Error Detection and Correction)** Controls FCM ECC functionality. • **'0' - Disabled NAND Flash ECC [Default]** • '1' - Enabled NAND Flash ECC

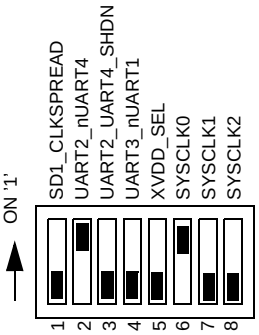
SW2 Configuration	
	**SW2.1 – SW2.6: SerDes MUX Configuration** Controls SerDes MUX routing; see *Hydra DS SERDES Support* and *P5040 DS Serdes Support.* • LANE_23_SEL: Selects routing of LANES[2:3]: **'0' - SLOT4 [Default for P3041/P5020]** **'1' - SLOT7 [Default for P5040]** • LANE_45_SEL: Selects routing of LANES[4:5] **'0' - SLOT6 [Default]**, '1' - SLOT7 • LANE_67_SEL[0:1]: Selects routing of LANES[6:7] – **'00' - SLOT5 [Default for P5040]** – **'10' - SLOT6 [Default for P3041/P5020]** – '01' - SLOT7 – '11' - NA • LANE_8_SEL: Selects routing of LANE[8]: **'0' - AURORA [Default for P3041/P5020]** **'1' - SLOT3 [Default for P5040]** • LANE_1617_SEL: Selects routing of LANES[16:17]: **'0' - SATA [Default for P3041/P5020]** **'1' - SLOT1 [Default for P5040]** **SW2.7: EP_nRC** **(End Point_nRoot Complex)** Controls SLOT7—determines its use as a PEX RC or a PEX EP. • **'0' - SLOT7 as an RC [Default]** • '1' - SLOT7 as an EP **SW2.8: ENG_USE3** **(Engineering Use3)** [Future option] Defines functionality. • **'1' - Default** • '0' - Spare

SW3 Configuration

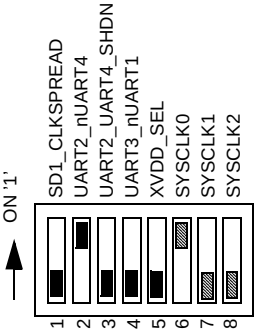
For P3041:



For P5020:



For P5040:



SW3.1: SD1_CLKSPREAD (SerDes Clock Spread)

Controls SERDES Bank1 clock spread spectrum modulation—determines if enabled or disabled.

- **'0' - SD1_CLKSPREAD disabled [Default]**
- '1' - Enabled SD1_CLKSPREAD

NOTE!

To use SERDES Bank1 spread spectrum modulation oscillator Y2 and R216 & R217 should be assembled while R213 & R214 - are disassembled.

SW3.2: UART2_nUART4 (Universal Asynchronous Receiver/Transmitter)

- **'1' - P3041/P5020/P5040 UART2 connected to RS-232 DB9 TOP [Default]**
- '0' - P3041/P5020/P5040 UART4 connected to RS-232 DB9 TOP

SW3.3: UART2_UART4_SHDN (UART_Shutdown)

- **'0' - Active UART2/UART4 connected to RS-232 DB9 TOP [Default]**
- '1' - UART2/UART4 in shutdown mode

SW3.4: UART3_nUART1 (Universal Asynchronous Receiver/Transmitter)

Controls P3041/P5020/P5040 UART3/UART1 Flow Control—determines if connected to RS-232 DB9 BOTTOM; see SW5.7 – SW5.8 description.

- **'0' - P3041/P5020/P5040 UART1 Flow Control (RTS, CTS) connected to RS-232 DB9 BOTTOM [Default]**
- '1' - P3041/P5020/P5040 UART3 connected to RS-232 DB9 BOTTOM.

SW3.5: XVDD_SEL (Select XVDD Voltage)

Controls XVDD voltage.

- **'0' - XVDD = 1.8V [Default]**
- '1' - XVDD = 1.5V

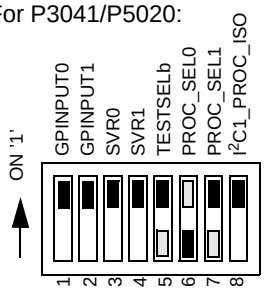
SW3.6 – SW3.8: SYSCLK[0:2] (System Clock Select)

Selects SYSCLK[0:2] speed as listed below:

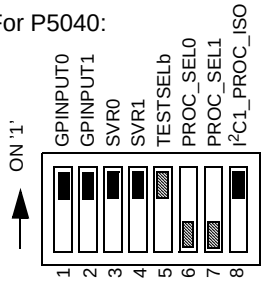
- '000' - 66.666 MHz
- '001' - 83.333 MHz **[Default for P3041]**
- '010' - 100 MHz
- '100' - 133.333MHz **[Default for P5040]**
- '011' - 125 MHz
- '100' - 133.333 MHz **[Default for P5020]**
- '101' - 150 MHz
- '110' - 160 MHz
- '111' - 166.666 MHz

SW4 Configuration

For P3041/P5020:



For P5040:



SW4.1– SW4.2: GPINPUT[0:1] (General Purpose Input)

Overwrites PLL settings when CFG_PLL_CONFIG_SEL_B = 1'b0.

- **'11' - Default**

SW4.3 – SW4.4: SVR [0:1] (System Version Register)

Defines system version register [0:1].

- '00' - Reserved
- '01' - Reserved
- '10' - Reserved
- **'11' - P5040/P3041/P5020/P4080 [Default]**

SW4.5: TESTSELb (Test Select)

Defines functionality.

- '0' - for P3041/P5021/P5010
- '1' - for P5040/P5020/P4080

SW4.6 – SW4.7: PROC_SEL[0:1] (Processor Select)

Combined with SW11.5 defines processor type:
SW11.5, SW4.7 ,SW4.6, = Processor type[2:0].
For detailes see the Table below.

SW11.5	SW4.7	SW4.6	Processor Type
0	0	0	P4080
0	0	1	P3041
0	1	0	P5020
0	1	1	P2040
1	0	0	P5040
1	0	1	P5010
1	1	0	P5021
1	1	1	Reserved

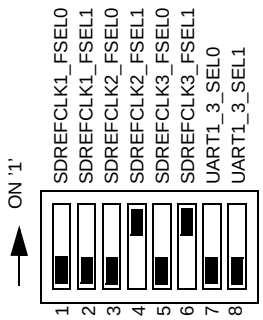
SW4.8: I2C1_PROC_ISO (Processor Isolated)

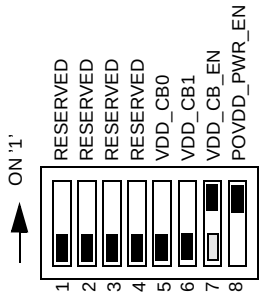
Controls CPU access to I2C1 connected devices: I2C RCW EEPROM, SYSTEM Configuration DATA EEPROM, DC-to-DC power supplies for CPU CA, CB, PL, and GVDD voltages.

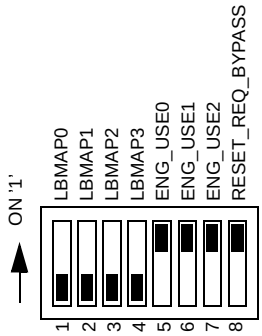
- 0 - CPU cannot access devices
- **1 - CPU accesses [Default]**

NOTE!

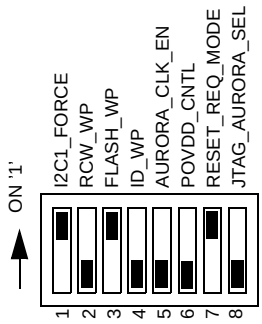
If SW8.1 = '1' then the CPU can access the EEPROM FPGA ExConfiguration Data.

SW5 Configuration	
	**SW5.1 – SW5.2: SDREFCLK1_FSEL[0:1]** **(SerDes Reference Clock Bank1 Frequency Select)** Selects SerDes reference clock for bank1[0:1]. • '00' -100 MHz **[Default]** • '01' - 125 MHz • '10' - 156.25 MHz • '11' - 212.5 MHz; unsupported by P3041/P5020/P5040 **SW5.3 – SW5.4: SDREFCLK2_FSEL[0:1]** **(SerDes Reference Clock Bank2 Frequency Select)** Selects SerDes reference clock for bank2[0:1]. • '00' - 100 MHz • '01' - 125 MHz **[Default]** • '10' - 156.25 MHz • '11' - 212.5 MHz; unsupported by P3041/P5020/P5040 **SW5.5 – SW5.6: SDREFCLK3_FSEL[0:1]** **(SerDes Reference Clock Bank3 Frequency Select)** Selects SERDES Reference Clock for Bank3[0:1]. • '00' - 100 MHz • '01' - 125 MHz **[Default]** • '10' - 156.25 MHz • '11' - 212.5 MHz; unsupported by P3041/P5020/P5040 **SW5.7 – SW5.8: UART1_3_SEL[0:1]** **(UART Connection Select)** Controls UART1 and UART3 connectivity options[0:1]. • **'00' - UART1 is connected to RS-232 DB9 BOTTOM; Selects UART1 with flow control if SW3.4: UART3_nUART1='0'. [Default]** – Selects UART1 without flow control if SW3.4: UART3_nUART1='1'. • '01' - UART3 or Reserved – Connects UART3 to RS-232 DB9 BOTTOM if SW3.4: UART3_nUART1='1' – Reserved if SW3.4: UART3_nUART1='0'. • '10' - Connects FPGA to RS-232 DB9 BOTTOM; the UART processor is not used. • '11' - Reserved

SW6 Configuration	
	**SW6.1– SW6.4: RESERVED** **SW6.5 – SW6.6: VDD_CB[0:1]** **(Core B Voltage)** [Optional] Defines additional core B voltage[0:1]. • **'00' - HW defined by switch SW10[3:4] [Default]** • '01' - Reserved (1.00V) • '10' - 1.05V • '11' - Reserved (1.15V) **SW6.7: VDD_CB_EN** **(Core B Voltage Enabled)** Controls Core B voltage—determines if enabled or disabled. • '0' - Disabled core B voltage [for P3041] • '1' - Enabled core B voltage [for P5020/P5040] **SW6.8: POVDD_PWR_EN** **(POVDD Voltage Enabled)** Controls POVDD power—determines if enabled or disabled. • '0' - Disabled POVDD power supply • **'1' - Enabled POVDD power supply [Default]**

SW7 Configuration	
	**SW7.1 – SW7.4: LBMAP[0:3]** **(Local Bus Map)** Controls local bus chip select options. • **'0000' - LCS0=NOR #0, LCS1=PJET, LCS2/4/5/6=NAND [Default]** • '0001' - LCS0=NOR #1, LCS1=PJET, LCS2/4/5/6=NAND • '0010' - LCS0=NOR #2, LCS1=PJET, LCS2/4/5/6=NAND • '0011' - LCS0=NOR #3, LCS1=PJET, LCS2/4/5/6=NAND • '0100' - LCS0=NOR #4, LCS1=PJET, LCS2/4/5/6=NAND • '0101' - LCS0=NOR #5, LCS1=PJET, LCS2/4/5/6=NAND • '0110' - LCS0=NOR #6, LCS1=PJET, LCS2/4/5/6=NAND • '0111' - LCS0=NOR #7, LCS1=PJET, LCS2/4/5/6=NAND • '1000' - LCS0=PJET, LCS1=NOR, LCS2/4/5/6=NAND • '1001' - LCS0/4/5/6=NAND, LCS1=PJET, LCS2=NOR • '1010'-'1111' - Reserved **SW7.5 – SW7.7: ENG_USE[0:2]** **(Engineering Use)** [Future option] Defines functionality. • **'111' - Default** **SW7.8: RESET_REQ_BYPASS** **(Reset Request Bypass)** Defines functionality. • '0' - Reset request is ignored • **'1' - Action defined by RESET_REQUEST_MODE SW8.7. [Default]**

SW8 Configuration



SW8.1: I²C1_Force

Controls CPU access to I²C1 connected devices owned by ngPIXIS device: FPGA as well as EEPROM FPGA Configuration Data and EEPROM ExConfiguration Data.

- 0 - System cannot access devices
- **1 - System can access devices [Default]**

NOTE!

If SW4.8 = '1' then the CPU accesses above noted devices.

SW8.2: RCW_WP (RCW Write Protect)

Defines RCW EEPROM WP.

- **'0' - No EEPROM WP [Default]**
- '1' - EEPROM WP

SW8.3: FLASH_WP (Flash Write Protect)

Defines NOR Flash and SPI Flash memory WP.

- '0' - NOR Flash and SPI Flash memory WP
- **'1' - No NOR Flash and SPI Flash memory WP [Default]**

SW8.4: ID_WP (ID Write Protect)

Defines EEPROM FPGA Configuration Data WP.

- **'0' - No EEPROM WP [Default]**
- '1' - EEPROM WP

SW8.5: AURORA_CLK_EN (Aurora Clock Enabled)

- Reserved; not used in P5040/P3041/P05020DS

SW8.6: POVDD_CNTL (POVDD Control)

Controls POVDD voltage.

- **'0'** - POVDD=1.5V Ready; **[Default]**
- '1' - POVDD = 1.0V Ready;

SW8.7: RESET_REQ_MODE (Reset Request Mode)

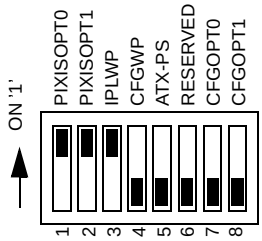
Defines reset request mode only if SW7.8 = '1'.

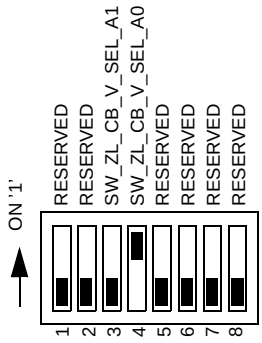
- '0' - RESET_REQ asserts HRESET to processor and resets system
- **'1'- RESET_REQ asserts PORESET to processor and resets system [Default]**

SW8.8: JTAG_AURORA_SEL (JTAG or Aurora Select)

Controls P5040/P3041/P5020 JTAG port access to COP/JTAG or Aurora connectors.

- **'0' - P5040/P3041/P5020 JTAG port connects to COP/JTAG connector [Default]**
- '1' - P5040/P3041/P5020 JTAG port connects to Aurora connector

SW9 Configuration	
	**SW9.1 – SW9.2: PIXISOPT[0:1] (ngPIXIS Option)** Controls OCM/DCM ngPIXIS options. • PIXISOPT[0] = '0' - Enabled debugger • **PIXISOPT[0] = '1' - Disabled debugger [Default]** • **PIXISOPT[1] = unused; '1' - [Default]** **SW9.3: IPLWP (IPL Write Protect)** Defines EEPROM FPGA ExConfiguration Data WP. • '0' - No EEPROM WP • **'1' - EEPROM WP [Default]** **SW9.4: CFGWP (Configuration Write Protect)** Defines EEPROM FPGA Configuration Data WP. • **'0' - No EEPROM WP [Default]** • '1' - EEPROM WP **SW9.5: ATX-PS (ATX Power Supply)** Defines if system automatically Powers-ON after ATX power supply is set to ON. • **'0' - ATX-PS is turned on but the board remains OFF; then press the power switch. [Default]** • '1' - Board powers automatically after ATX-PS is turned ON. **SW9.6: RESERVED** **SW9.7: CFGOPT[0] - DCM SHELL** • **'0' - DCM works in background [Default]** • '1' - DCM interacts over COM1 Port **SW9.8: CFGOPT[1] - DCM DIS** • **'0' - DCM inhibited (GMSA forced into RESET) [Default]** • '1' - DCM operational (GMSA runs)

SW10 Configuration:	
	**SW10.1– SW10.2: RESERVED** **SW10.3 – SW10.4: SW_ZL_CB_V_SEL_A[1:0] (Software Core B Voltage Select)** Defines core B voltage. • '00' - 1.0V; • **'01' - 1.1V; [Default]** • '10' - 1.2V • '11' - 0.9V **SW10.5 – SW10.8: RESERVED**

SW11 Configuration:

For P3041/P5020:

For P5040:

SW11.1– SW11.4: PDN_CFG[0:3] (Power Switches Configuration)

Defines PDN Power Switches control signals.
Details described in the Table Below.

- **'0000' - Independent; [Default for P5020]**
- **'0011' - CA+CB - Common; PL - Independent; [Default for P5040]**
- **'0010' - PL+CA+CB=Common; [Default for P3041]**
- **'0110' - PL, CA - Independent; CB - Disconnected; [Default for P5021]**
- **'0101' - PL+CA = Common; CB - Disconnected; [Default for P5010]**

SW11.1	SW11.2	SW11.3	SW11.4	PDN Config
0	0	0	0	Independent
0	0	0	1	PL+CA=Common; CB-Independant
0	0	1	0	PL+CA+CB=Common
0	0	1	1	CA+CB=Common; PL-Independant
0	1	0	0	Reserved
0	1	0	1	PL+CA=Common; CB-Disconnected
0	1	1	0	PL,CA=Independent; CB-Disconencted
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	PL-OFF; DUT not Powered

SW11.5: PROC_SEL2 (Processor Select)

Combined with SW4.7-SW4.6 defines processor type [2:0].
For detailes see description in SW4.6-SW4.7

- **'0' - Default for P3041/P5020**
- **'1' - Default for P5040/P5021/P5010**

SW11.6: LANE_9_SEL

Controls SerDes MUX routing of LANE_9_SEL:

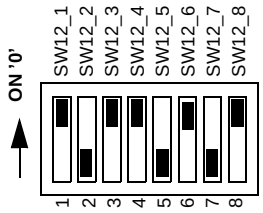
- **'1' - AURORA [Default for P3041/P5020]**
- **'0' - SLOT3 [Default for P5040]**

SW11.7 – SW11.8: SDREFCLK4_FSEL[0:1] (SerDes Reference Clock Bank4 Frequency Select)

Selects SerDes reference clock for P5040 bank4 [0:1] only;
not relevant for P3041/P5020.

- '00' -100 MHz
- '01' - 125 MHz **[Default]**
- '10' - 156.25 MHz
- '11' - 212.5 MHz;

SW12 Configuration:



SW12.1– SW12.8: VDD_CA_VOLT_SET
(VDD_CA voltage set)

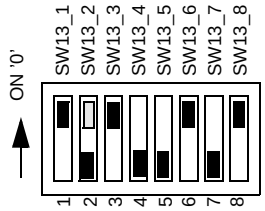
Defines VR11 Intel Mode voltage identification codes for VDD_CA.
See *Intersil ISL6313B* data sheet.
SW12[1:8] = U135 ISL6313B[VID0:VID7]
Details described in the Table Below.

- **'01001010' - SW12[1:8], 1.10000V; [Default]**

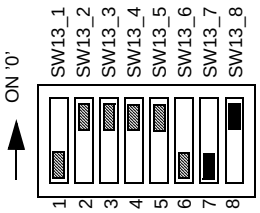
SW12.8	SW12.7	SW12.6	SW12.5	SW12.4	SW12.3	SW12.2	SW12.1	VDAC
0	0	0	X	X	X	X	X	Unallowed
0	0	1	X	X	X	X	X	Unallowed
0	1	0	0 ⋮ 1	0 ⋮ 1	0 ⋮ 1	0 ⋮ 1	0 ⋮ 1	1.21250V ⋮ 1.01875V
0	1	1	0 ⋮ 1	0 ⋮ 1	0 ⋮ 1	0 ⋮ 1	0 ⋮ 1	1.01250V ⋮ 0.81875V
1	X	X	X	X	X	X	X	Power OFF

SW13 Configuration:

For P5020/P3041



For P5040



SW13.1– SW13.8: VDD_PL_VOLT_SET
(VDD_PL voltage set)

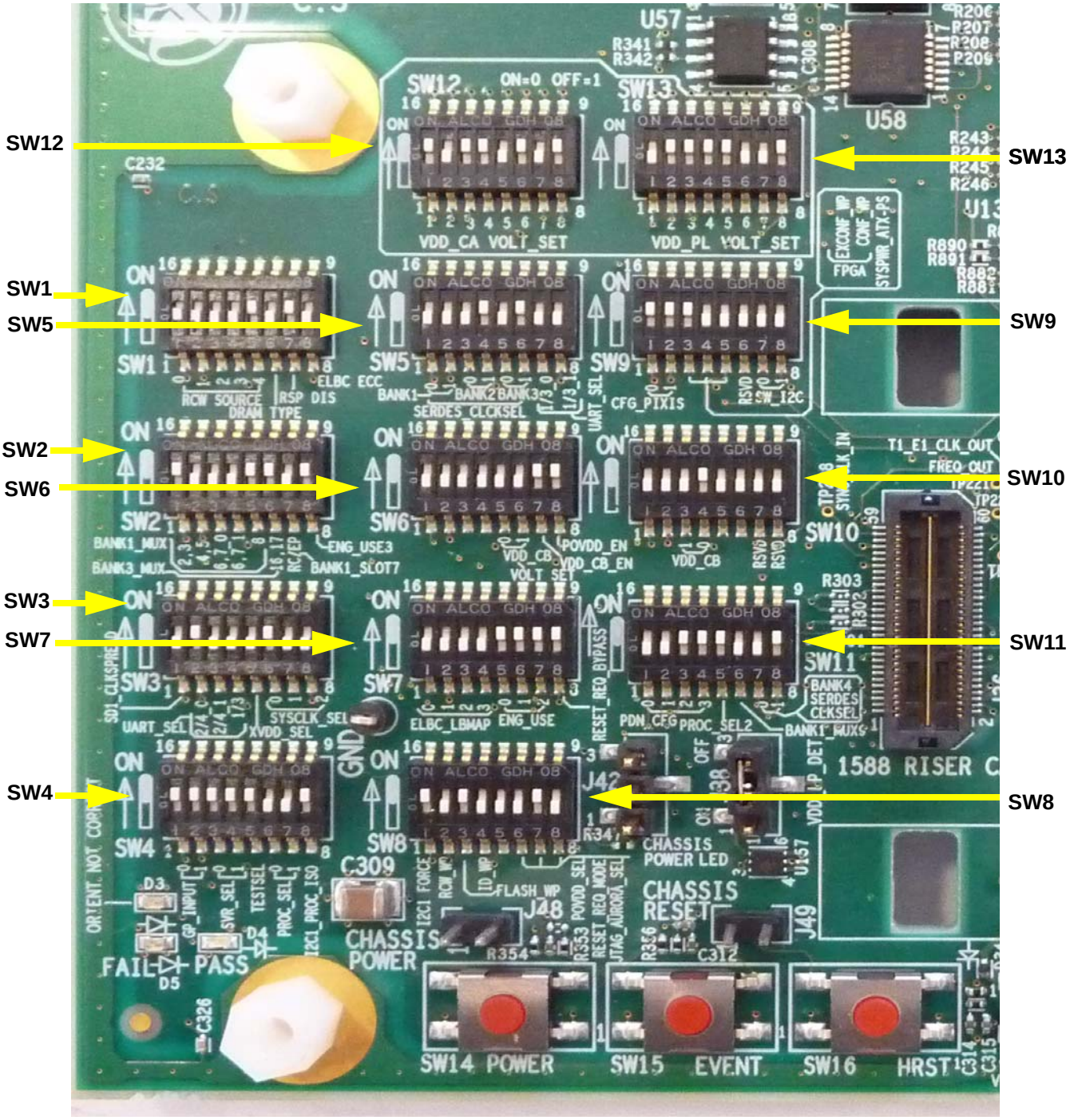
Defines VR11 Intel Mode voltage identification codes for VDD_PL.
See *Intersil ISL6313B* data sheet.
SW13[1:8] = U147 ISL6313B[VID0:VID7]
Details described in the Table Below.

- **'01011010' - SW13[1:8], 1.05000V; [Default for P5020]**
- **'00011010' - SW13[1:8], 1.06250V; [Default for P3041]**
- **'10000110' - SW13[1:8], 1.00625V; [Default for P5040]**

SW13.8	SW13.7	SW13.6	SW13.5	SW13.4	SW13.3	SW13.2	SW13.1	VDAC
0	0	0	X	X	X	X	X	Unallowed
0	0	1	X	X	X	X	X	Unallowed
0	1	0	0 • • • 1	0 • • • 1	0 • • • 1	0 • • • 1	0 • • • 1	1.21250V • • • 1.01875V
0	1	1	0 • • • 1	0 • • • 1	0 • • • 1	0 • • • 1	0 • • • 1	1.01250V • • 0.81875V
1	X	X	X	X	X	X	X	Power OFF

Figure 4 shows DIP-switch location.

Figure 4. P5040 DS (SuperHYDRA) DIP-Switch Locations



7 Connector Default Settings

Table 6 lists factory default connector settings for P5040 DS (SuperHYDRA). Figure 5 notes connector locations.

Table 6. P5040 DS (SuperHYDRA) Connector Default Settings

Connector	Name/Function	Type	Features	Description
J1	USB2 OTG	Micro-AB USB	9-pin	**[Default] OPEN**
J2	• GETH1 • USB1 Host	• RJ-45 • USB Type-A	• RJ-45: 12-pin • USB Type-A: 4-pin	**[Default] OPEN**
J3	SD/eMMC Card Slot	Socket	19-pin	**[Default] No inserted SD/eMMC card**
J5	Dual RS-232: • UART1/3-Bottom • UART2/4-Top	DB9 RS-232	Dual 9-pins	External RS-232 adapter cable connection
J6	SLOT-1 Sideband	Socket	2x20-pin	For SGMII/XAUI riser card
J7	SLOT-2 Sideband	Socket	2x20-pin	For SGMII/XAUI riser card
J53	SLOT-3 Sideband	Socket	2x20-pin	For SGMII riser card
J8	SLOT-5 Sideband	Socket	2x20-pin	For SGMII riser card
J9	SLOT-6 Sideband	Socket	2x20-pin	For SGMII riser card
J10	SLOT-7 Sideband	Socket	2x20-pin	Reserved
J12	UART service	Header	1x3-pin	**Not assembled**
J13	SATA1	SATA	7-pin	External SATA cable connection
J14	SATA2	SATA	7-pin	External SATA cable connection
J16	I^2C2 remote programmer	Header	1x3-pin	External I^2C2 remote programmer connection
J19	External system clock source	SMB COAX	—	**[Default] OPEN**
J20	PEX SLOT-1	PEX Socket	164-pin	**[Default] OPEN**
J21	PEX SLOT-2	PEX Socket	164-pin	**[Default] OPEN**
J22	PEX SLOT-3	PEX Socket	164-pin	**[Default] OPEN**
J23	PEX SLOT-4	PEX Socket	164-pin	**[Default] OPEN**
J24	PEX SLOT-5	PEX Socket	164-pin	**[Default] OPEN**
J25	PEX SLOT-6	PEX Socket	164-pin	**[Default] OPEN**
J26	PEX SLOT-7	PEX Socket	164-pin	**[Default] OPEN**

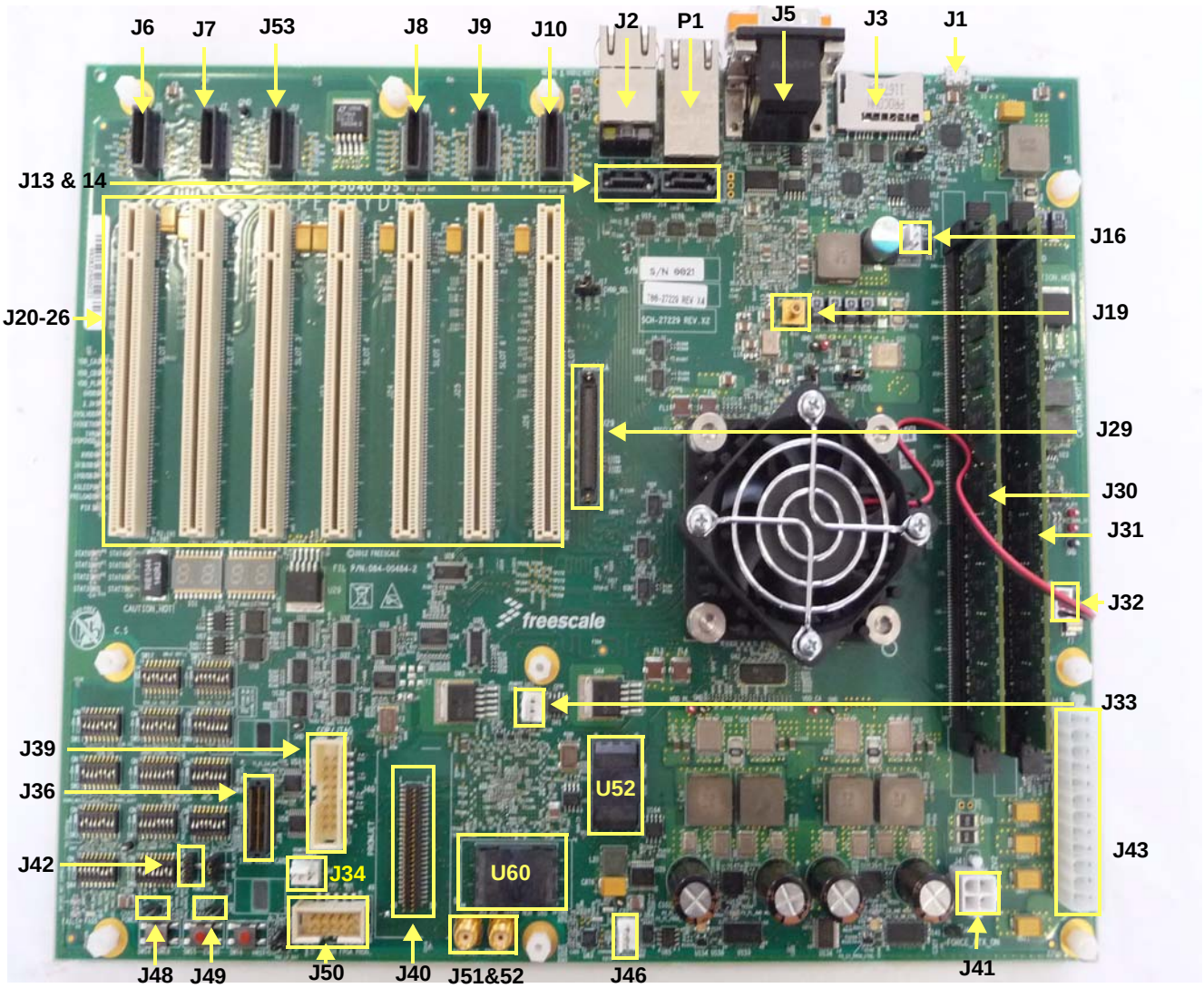
Table 6. P5040 DS (SuperHYDRA) Connector Default Settings

Connector	Name/Function	Type	Features	Description
J29	AURORA	AURORA Socket	2x35-pin	External AURORA cable connection
J30	DDR3 DIMM1	DDR3 uDIMM Socket	240-pin	uDIMM-2GB 72bit (with ECC) 1600Mbps Dual Rank inserted **[For P3041/P5020/P5040]**
J31	DDR3 DIMM2	DDR3 uDIMM Socket	240-pin	uDIMM-2GB 72bit (with ECC) 1600Mbps Dual Rank inserted **[Not Used for P3041]**
J32	CPU FAN	Header	1x3-pin	12V FAN
J33	I^2C1 isolated bus remote programmer	Header	1x3-pin	External I^2C1 remote programmer connection
J34	I^2C4 bus remote programmer	Header	1x3-pin	External I^2C4 remote programmer connection
J35	12V	Header	1x2-pin	**Not assembled**
J36	1588 riser card	Header	2x30-pin	External 1588 riser card connection
J39	JTAG/COP	Header	2x8-pin	External USB-TAP connection
J40	PROMJet	Header	2x25-pin	External PROMJet Flash emulator connection
J41	ATX-PS 12V2	Connector	2x2-pin	External ATX-PS 12V connection
J42	Chassis power LED	Header	1x3-pin	PC box chassis power (VCC_3V3) LED connection
J43	ATX-PS	Connector	2x12-pin	External ATX-PS connection
J45	System test	Header	1x2-pin	• Voltage monitor service disconnection. • **Not assembled**
J46	I^2C1 Zilker converters remote programmer	Header	1x3-pin	External I^2C1 remote programmer connection
J48	Chassis power LED	Header	1x3-pin	PC box chassis power (VCC_HOT3V3) LED connection
J49	Chassis reset LED	Header	1x3-pin	PC box chassis reset LED connection
J50	Flash FPGA programming	Header	2x5-pin	**[Default] OPEN**
J51	TRIG_OUT	SMA COAX	—	**[Default] OPEN**
J52	TRIG_IN	SMA COAX	—	**[Default] OPEN**

Table 6. P5040 DS (SuperHYDRA) Connector Default Settings

Connector	Name/Function	Type	Features	Description
P1	GETH2	RJ-45	12-pin	**[Default] OPEN**
U52	NAND Flash socket	Socket	48-pin	8GBit NAND Flash inserted
U60	NOR Flash socket	Socket	56-pin	1GB NOR Flash inserted

Figure 5. Super Hydra Connectors



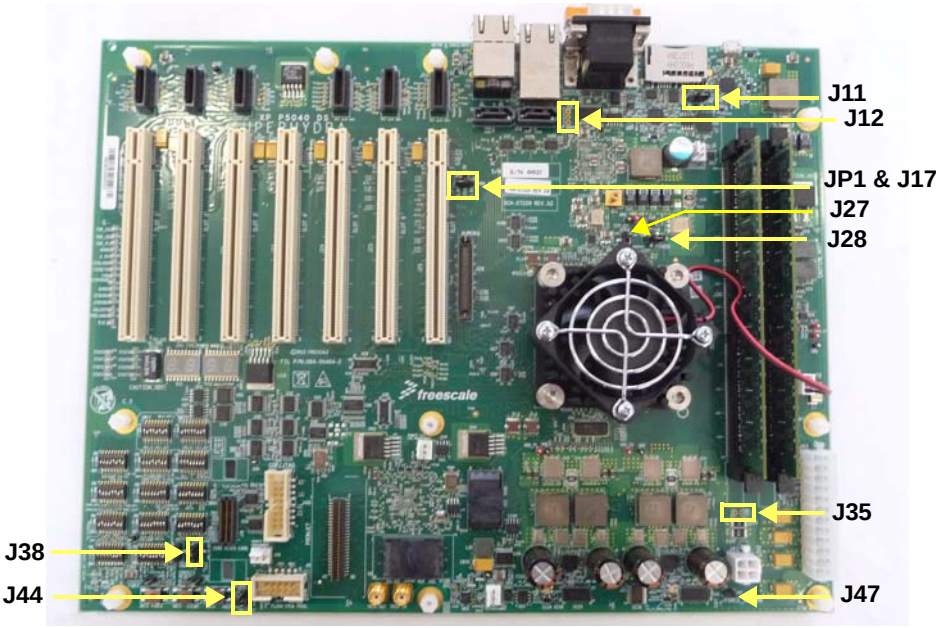
8 Jumper Default Settings

Table 7 lists factory default jumper settings for P5040 DS (SuperHYDRA). Figure 6 notes jumper locations.

Table 7. P5040 DS (SuperHYDRA) Jumper Default Settings

Jumper	Type	Features	Name/Function	Description
J11	Header	1x3-pin	SD/eMMC card detect selection	• **1-2: [Default] eSDHC mode** • 2-3: eMMC mode
J17, JP1	Combined Headers	1x3-pin & 1x1-pin	CVDD selection	• **1-2: [Default] 3.3V** • 2-3: 1.8V • 2-4: 2.5V
J27	Header	1x3-pin	System clock source selection	• 1-2: External SYSCLK • **2-3: [Default] onboard SYSCLK**
J28	Header	1x3-pin	POVDD selection	• 1-2: ON • **2-3: [Default] OFF**
J38	Header	1x3-pin	VDD LP detection	• 1-2: ON; • **2-3: [Default] OFF**
J44	Header	1x2-pin	VDD LP battery selection	• Connected: Enabled VDD_LP_BAT • **Disconnected [Default]: Disabled VDD_LP_BAT**
J47	Header	1x2-pin	Force ATX-ON	• Connected: Force ATX-PS ON • **Disconnected [Default]: Normal operation**

Figure 6. Super Hydra Jumper Locations



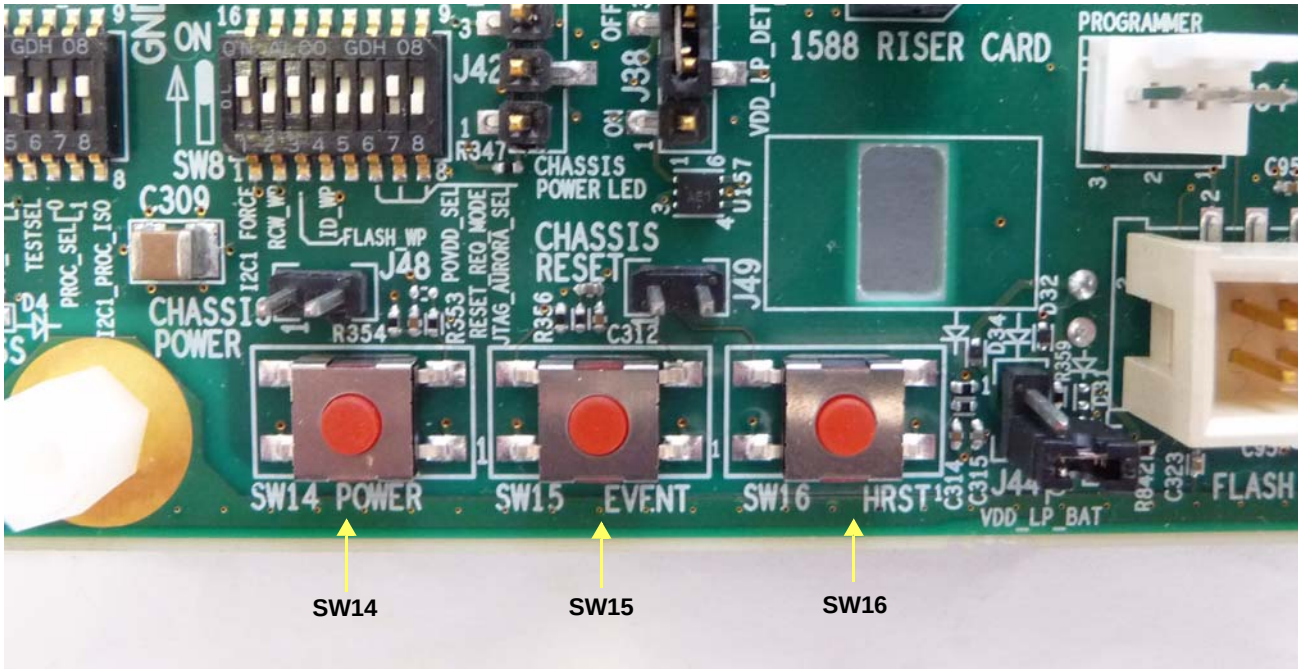
9 Push Buttons

Table 8 lists the functioning of P5040 DS (SuperHYDRA) push buttons. Figure 7 notes push button locations.

Table 8. P5040 DS (SuperHYDRA) Push Buttons

Push Button	Function	Description
SW14	Power (ON/OFF)	• Press SW14 to assert Power-ON/OFF. • Powered by an external ATX power supply via J43 and J41 power connectors. • System automatically powers-on after asserting ATX power supply if SW9.5=’1’.
SW15	Event	• Press SW15 to issue processor IRQ4.
SW16	Hard Reset (HRST)	• Press SW16 for Hard Reset.

Figure 7. Super Hydra Push Button Locations



10 LED Lights

Figure 8, below, lists the functioning of SuperHYDRA LED lights. See Table 9 for LED locations.

Table 9. P5040 DS (SuperHYDRA) LEDs

LED	Color	Name	LED ON	LED OFF
D3	Red	ORIENT NOT CORRECT	• Incorrect processor orientation in the socket	• Correct processor orientation in the socket
D4	Blue	PASS	One of the following: • Successful FPGA initialization; correct processor orientation; and all on-board voltage is in good condition • Register bit PX_CSR[7]='0'	One of the following: • Power Off • Unsuccessful FPGA initialization • Incorrect processor orientation • Some/all of on-board voltage is in poor condition • Register bit PX_CSR[7]='1'
D5	Red	FAIL	One of the following: • Unsuccessful FPGA initialization • Incorrect processor orientation • Some/all of on-board voltage is in poor condition • Register bit PX_CSR[7]='1'	One of the following: • Power Off • Successful FPGA initialization; correct processor orientation; and all on-board voltage is in good condition • Register bit PX_CSR[7]='0'
D6	Green	STAT0	• Reset: lighted if LB_CS0_b='0' (BOOT) • Normal operation: lighted if register bit PX_LED[0]='1'	• Register bit PX_LED[0]='0'
D7	Green	STAT1	• Reset: lighted if LB_CS1_b='0' • Normal operation: lighted if register bit PX_LED[1]='1'	• Register bit PX_LED[1]='0'
D8	Green	STAT2	• Reset: lighted if I^2C1_SCL or I^2C4_SCL are non-existent • Normal operation: lighted if register bit PX_LED[2]='1'	• Register bit PX_LED[2]='0'
D9	Green	ASLEEP	• Asserted: P3041/P5020 HRESET	• P3041/P5020 HRESET unasserted
D10	Green	STAT3	• Reset: lighted if ASLEEP is present • Normal operation: lighted if register bit PX_LED[3]='1'	• Register bit PX_LED[3]='0'
D11	Green	STAT4	• Normal operation: lighted if register bit PX_LED[4]='1'	• Register bit PX_LED[4]='0'

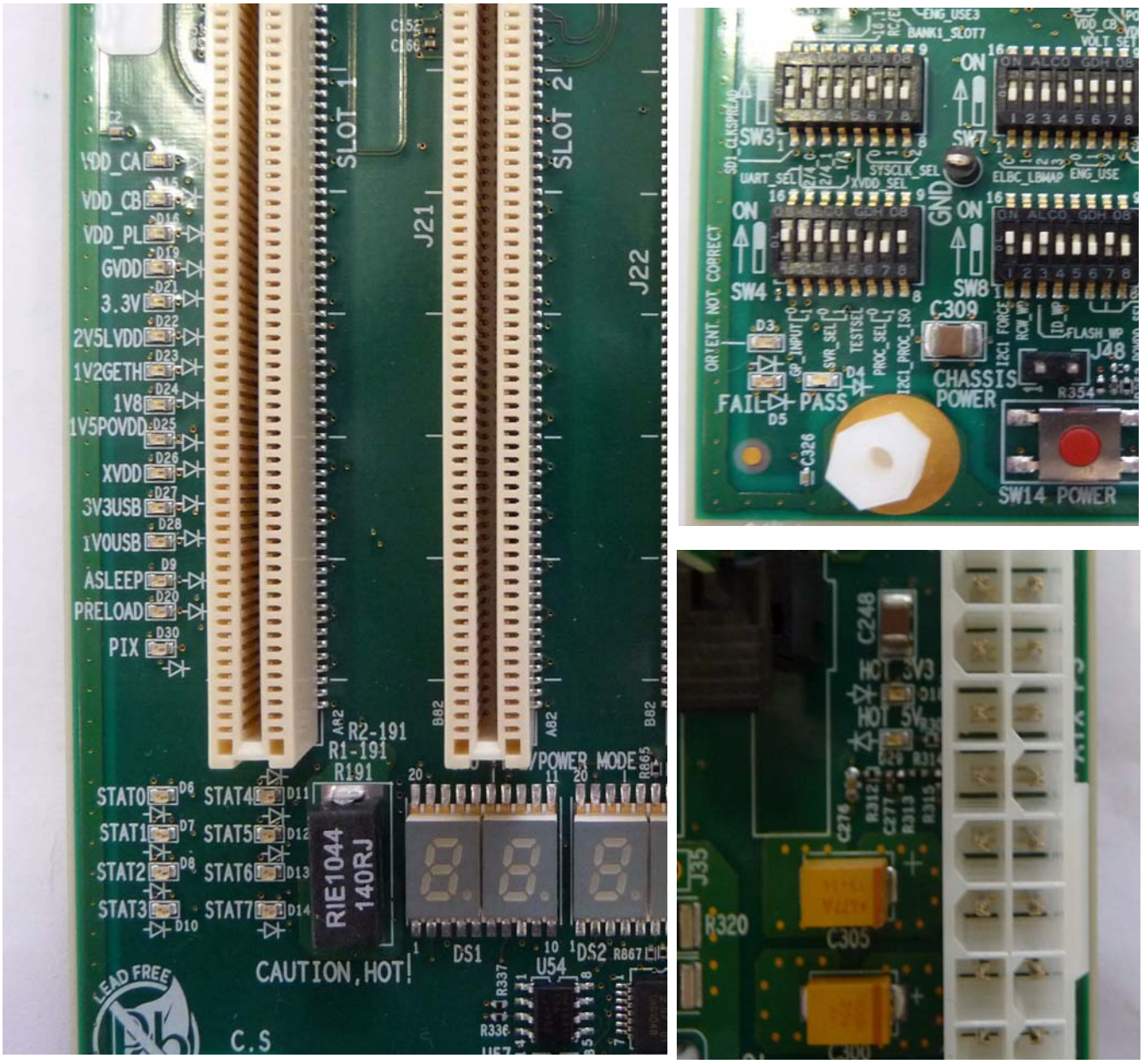
Table 9. P5040 DS (SuperHYDRA) LEDs

LED	Color	Name	LED ON	LED OFF
D12	Green	STAT5	• Reset: lighted if OCM initialization fails • Normal operation: lighted if register bit PX_LED[5]='1'	• Register bit PX_LED[5]='0'
D13	Green	STAT6	• Reset lighted if FPGA OCM is clocked • Normal operation: lighted if register bit PX_LED[6]='1'	• Register bit PX_LED[6]='0'
D14	Green	STAT7	• Flashes when FPGA is clocked • Normal operation: lighted if register bit PX_LED[7]='1'	• Register bit PX_LED[7]='0'
D15	Green	VDD_CB_PG	• Power Good: VDD_CB	• Failed: VDD_CB Power
D16	Green	VDD_PL_PG	• Power Good: VDD_PL	• Failed: VDD_PL Power
D17	Green	VDD_CA_PG	• Power Good: VDD_CA	• Failed/OFF for P3041: VDD_CA Power
D18	Green	HOT_3V3	• Power Good: HOT_3V3	• Failed: HOT_3V3 Power
D19	Green	VDD_GVDD_PG	• Power Good: VDD_GVDD	• Failed: VDD_GVDD Power
D20	Green	PRELOAD	• ON: PRELOAD	• OFF: PRELOAD status
D21	Green	3V3	• ON: 3.3V voltage supply	• OFF: 3.3V voltage supply
D22	Green	2V5LVDD	• ON: 2.5V LVDD voltage supply	• OFF: 2.5V LVDD voltage supply
D23	Green	1V2GETH	• ON: 1.2V GETH PHY Core voltage supply	• OFF: 1.2V GETH PHY Core voltage supply
D24	Green	1V8	• ON: 1.8V voltage supply	• OFF: 1.8V voltage supply
D25	Green	1V5POVDD	• ON: 1.5V POVDD voltage supply	• OFF: 1.5V POVDD voltage supply
D26	Green	XVDD	• ON: XVDD voltage supply	• OFF: XVDD voltage supply
D27	Green	3V3USB	• ON: 3.3V USB voltage supply	• OFF: 3.3V USB voltage supply
D28	Green	1V0USB	• ON: 1.0V USB voltage supply	• OFF: 1.0V USB voltage supply
D29	Green	HOT_5V	• ON: HOT_5V voltage supply	• OFF: HOT_5V voltage supply
D30	Green	PIX	• ON: FPGA OCM	• OFF: FPGA OCM
D35	Green	PS_CA_AMD MODE	• ON: PS_CA in AMD 5-bit mode	• OFF: PS_CA in Intel VR11 mode
D36	Green/ Red	PS_CA_PROG_ CNTR	• Green: Voltage set by SW12 • Red: Voltage set by I2C1 bus	• OFF: Power OFF
D37	Green	PS_PL_AMD MODE	• ON: PS_PL in AMD 5-bit mode	• OFF: PS_PL in Intel VR11 mode

Table 9. P5040 DS (SuperHYDRA) LEDs

LED	Color	Name	LED ON	LED OFF
D38	Green/ Red	PS_PL_PROG_ CNTR	• Green: Voltage set by SW13 • Red: Voltage set by I2C1 bus	• OFF: Power OFF

Figure 8. P5040 DS (SuperHYDRA) LED (D) Locations



11 Working Environment

Features of the working environment are outlined in Table 10.

Table 10. P5040 DS (SuperHYDRA) Working Environment

Mode	Components	Optional Expansion
Inside PC Box	• ATX12V • 250 GB hard disk • DVD R/W drive	• Plug SGMII riser card into PEX slots 1, 2, 3, 5, or 6. • Plug XAUI riser card into PEX slots 1 or 2.
Standalone	• ATX12V	• Plug SGMII riser card into PEX slots 1, 2, 3, 5, or 6. • Plug XAUI riser card into PEX slots 1 or 2.

NOTE!

ATX12V powers the P3041/P5020 DS via J41 and J43.

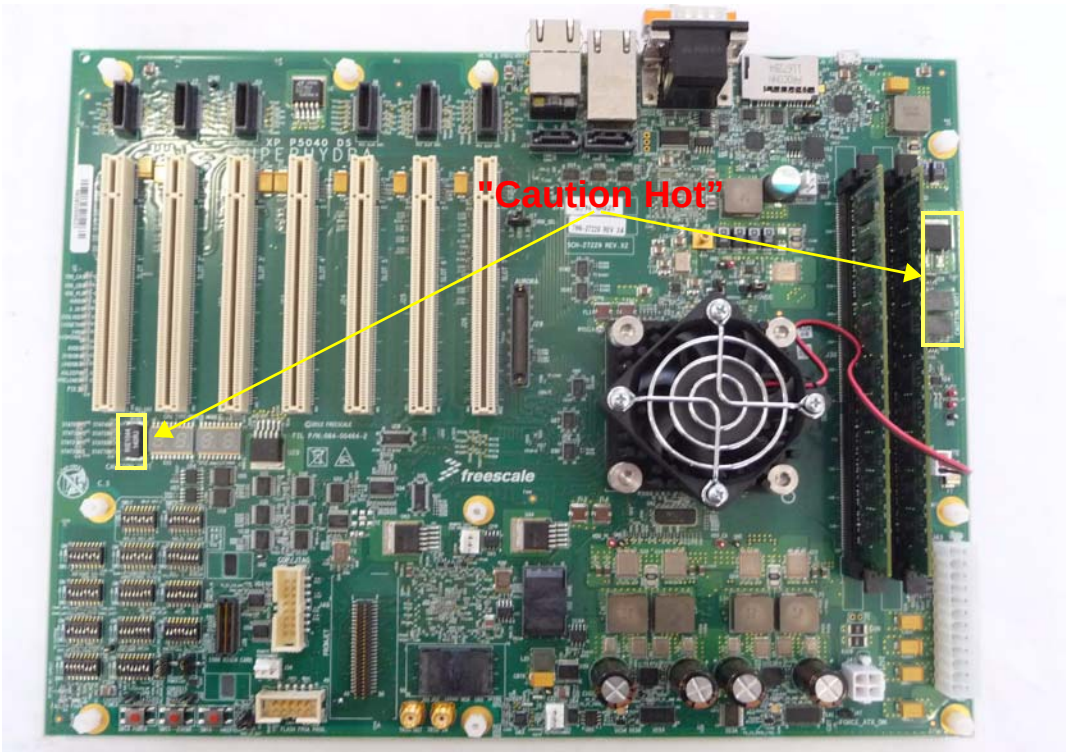
12 HW Getting Started Procedures

Table 11 outlines standalone activation of the P5040 DS (SuperHYDRA).

Additional HW options—not contained in the P5040 DS (SuperHYDRA) kit—include adding an SD/EMMC card, Aurora and PROMJet devices, and a 1588 riser card.

CAUTION!

The board is marked with several “Caution Hot” locations (R153, R173, R181, and R191); they are a consideration when the chip is in ‘Asleep’ mode and/or no processor is found on the board.



12.1 Standalone Mode

Table 11. Getting Started Procedure: Standalone Mode

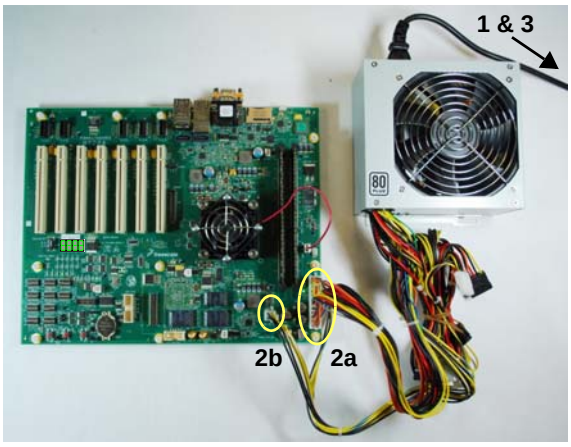
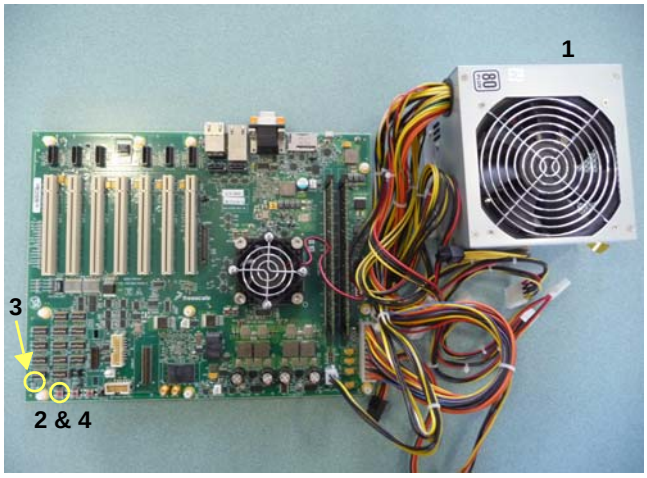
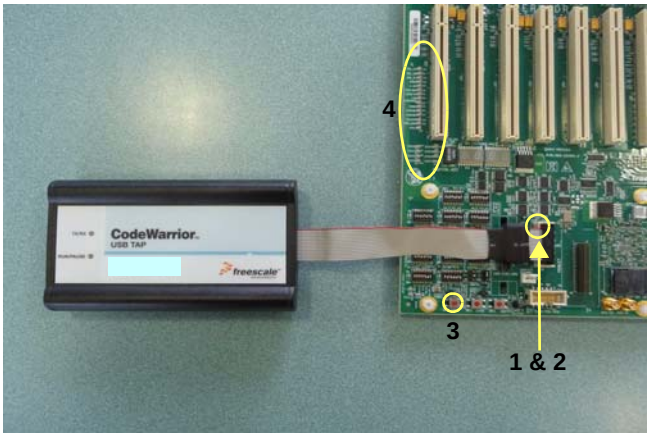
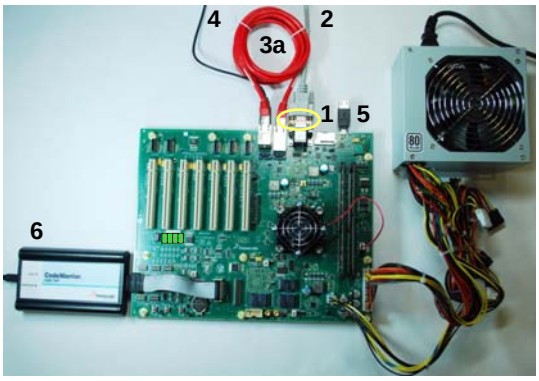
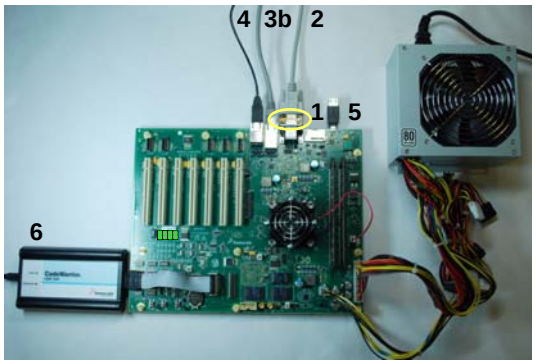
Getting Started Procedure: Standalone	
Step 1: Check HW kit contents.	**Section 4, "Hardware Kit Contents"**
Step 2: Check default SW settings.	**Section 6, "Switch Default Settings"**
Step 3: Check default connector settings.	**Section 7, "Connector Default Settings"**
Step 4: Check default jumper settings.	**Section 8, "Jumper Default Settings"**
Step 5: Establish working environment.	**Section 11, "Working Environment"**
Step 6: Assemble and connect ATX12V PS (standalone mode).	
NOTE! Ensure Power-OFF. 1. Assemble ATX12V PS kit: connect country-specific wall outlet plug to the primary power cable. 2. Connect the ATX12V PS harness to the board. a) Connect main power connector to J43. b) Connect +12V2DC connector to J41. 3. Plug the power cable into the wall outlet.	
Step 7: Perform initial board Power-ON and check LEDs.	
1. Power the board via the external ATX12V PS: LED D29 (HOT_5V) and D18 (HOT_3V3) will glow green. 2. Press SW14 to Power-ON. 3. Check for completion of Power-ON reset sequence as per LEDs D3:D30; see Section 10, "LED Lights". 4. Press SW14 to Power-OFF.	

Table 11. Getting Started Procedure: Standalone Mode

Getting Started Procedure: Standalone	
Step 8: Connect CW USB TAP.	
CAUTION! Avoid damage, follow the below steps. 1. Align the red stripe of the USB-UTAP connector cable with Pin 1 of the JTAG/COP 16-pin connector (at J39). 2. Connect the connector cable to J39. 3. Press SW14 to Power-ON. 4. Check for completion of the reset sequence (D3:30). **NOTE!** Freescale's CW USB TAP enables CW IDE software to work with P5040 DS (SuperHYDRA).	
Step 9: Attach cables per user development needs and planned board use.	
1. Ensure (pre-installed) DB9 Cross Gender adapter is connected to RS-232 J5-Bottom connector. 2. Connect between the DB9 Cross Gender adapter (J5-Bottom: UART 1/3) and the PC using an RS-232 standard serial cable. 3. Select and connect the appropriate Ethernet RJ45 cable. a) Connect cross-over cable between J2-Top–GETH1 and P1–GETH2; or, b) Connect shielded cable at J2-Top–GETH1 and/or P1–GETH2. **NOTE!** Only one shielded Ethernet RJ45 cable is included in the P5040 DS (SuperHYDRA) kit. 4. Connect USB*A-to-MicroUSB*B cable to J2-Bottom–USB1 (Host). 5. Connect MicroUSB*A-to-USB*A adapter to J1–USB2 (OTG). 6. Continue as per CW Kit Configuration Guide instructions.	 

12.2 PC Mid-Tower Mode

Table 12 outlines activation steps for a PC Mid-Tower unit.

Table 12. Getting Started Procedure: PC Mid-Tower Mode

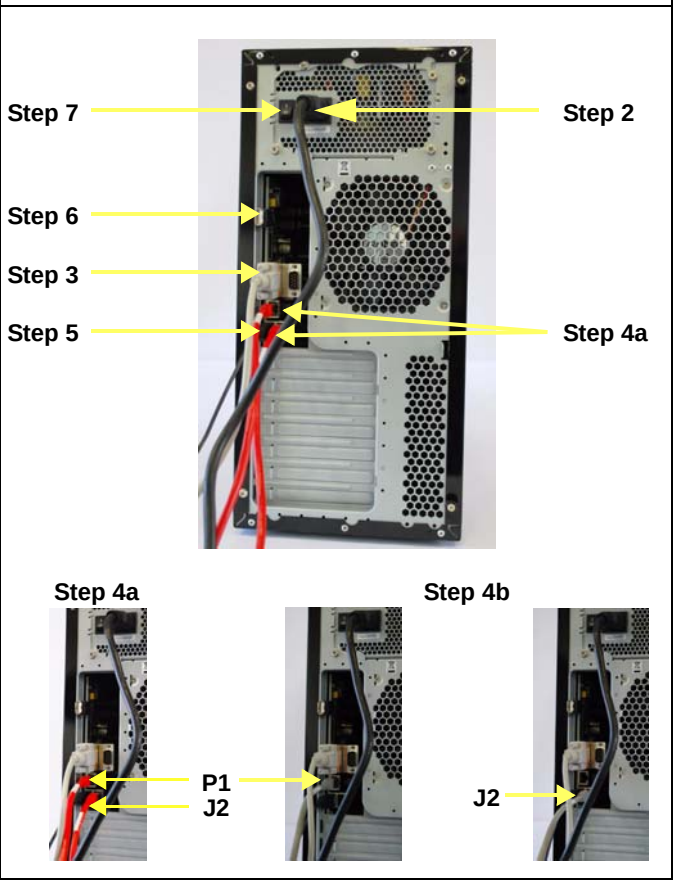
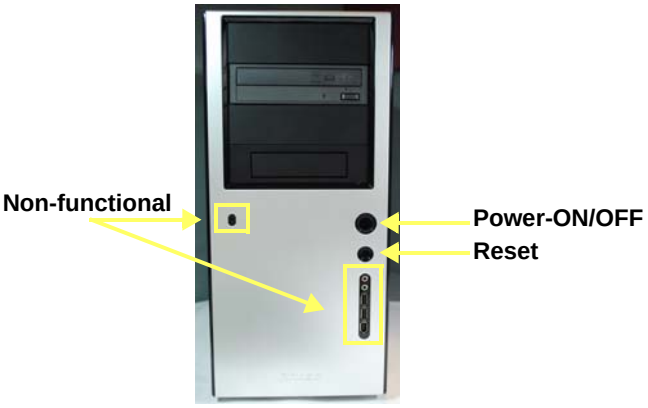
Getting Started Procedure: PC Mid-Tower	
Step 1: Attach country-specific wall outlet plug to the primary power cable.	
Step 2: Connect power cable to back of Mid-Tower unit.	
Step 3: Connect RS-232 cable to DB9 Cross Gender at J5-Bottom.	
Step 4a: Connect cross-over cable between P1–GETH2 and J2-Top–GETH1. **Step 4b:** Connect shielded cable at P1–GETH2 and/or J2-Top–GETH1.	
Step 5: Connect USB*A-to-MicroUSB*B cable to J2-Bottom–USB1 (Host).	
Step 6: Connect MicroUSB*A-to-USB*A adapter to J1–USB2 (OTG).	
Step 7: Set the power switch located on the back of the Mid-Tower to ON; it can remain in this position.	

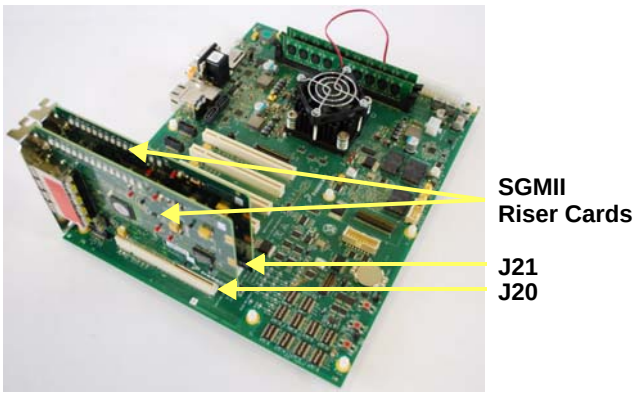
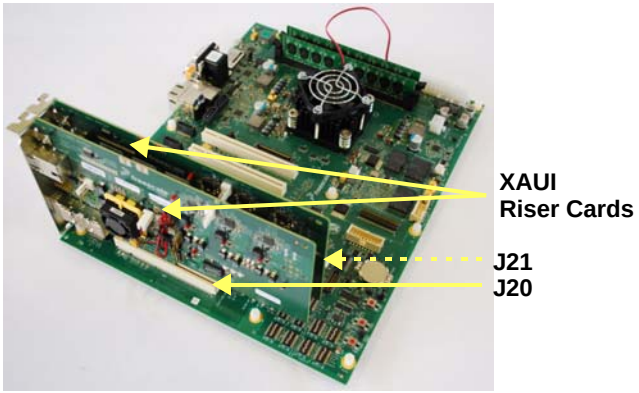
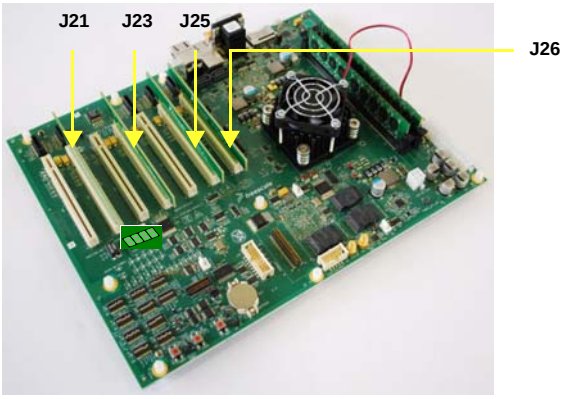
Table 12. Getting Started Procedure: PC Mid-Tower Mode

Getting Started Procedure: PC Mid-Tower	
Step 8: Power-ON: press the uppermost push button on the front panel of the Mid-Tower PC box. The lighted blue LED encircling the push button indicates power. **NOTE!** Plugs and USB ports located on the front panel of the Mid-Tower are not functional.	
Step 9: Power-OFF by pressing the same uppermost push button. Blue LED will shut off.	

13 SerDes Options

There are three SerDes module set-up options: SGMII and XAUI riser cards, and PEX loopback cards.

Table 13. SerDes Module Set-ups

SGMII Riser Card	
1. Select a configuration scenario; e.g., switch settings. 2. Connect the supplied cables as instructed in Section 12.1, "Standalone Mode". 3. Insert a SGMII riser card into slots J21, J22 and J24 for P5040 device or alternatively J20 and J21 for P3041/P5020 devices. 4. Press SW14 to Power-ON.	
XAUI Riser Card	
1. Select a configuration scenario; e.g., switch settings. 2. Connect the supplied cables as instructed in Section 12.1, "Standalone Mode". 3. Insert XAUI riser card into slots J20 and J21. 4. Connect a loopback cable between the two XAUI riser card connectors (S1/S2?) OR connect a cable to each XAUI riser card connector and an external destination. 5. Press SW14 to Power-ON.	
PEX Loopback	
1. Select a configuration scenario; e.g., switch settings. 2. Connect the supplied cables as instructed in Section 12.1, "Standalone Mode". 3. Insert PEX loopback cards in slots J25 and J26 for P5040 device or alternatively J21, J22, J23, J25 and J26 fro P3041/P5020 devices. 4. Press SW14 to Power-ON.	

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Japan
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+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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